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EXAMINER	
WANG, TED M	

ART UNIT	PAPER NUMBER
2634	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/010,819	MELANSON, JOHN LAWRENCE	
	Examiner	Art Unit	
	Ted M. Wang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 14-20* is/are rejected.

7)☒ Claim(s) *10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed on 10/03/2005, with respect to claim 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 6, 16, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Landry (US 5,931,891).

- With regard claim 1, Landry discloses a clock signal generator (digital frequency synthesizer) comprising:

  input circuitry (Fig.2 and 4 elements 10, 20, and 30, column 1 lines 45-59, and column 4 lines 38-44) for receiving an input signal (Fig.2 and 4 element 30 and column 1 lines 45-59) and a clock signal (Fig.2 and 4 elements 10 and column 1 lines 45-59) and generating a memory address therefrom (column 2 lines 15-21);

  a memory (Fig.2 element 40 and Fig.4 element 80, where the triangle wave is the combination of the sine wave that is well known in the art.) for storing digital data indexed by said memory address (column 2 lines 4-21) and

representing at least a portion of a substantially sinusoidal analog clock signal (Fig.2 element 40 and column 2 lines 4-21);

a digital to analog converter for converting data retrieved from said memory to generate said analog clock signal (Fig.2 and 4 element 50 and column 2 lines 22-34 and column 4 lines 62-64);

a filter for filtering the substantially sinusoidal analog clock (Fig.2 and 4 element 60 and column 2 lines 35-40 and column 5 lines 12-35) to reduce jitter in a binary clock signal derived therefrom (column 4 lines 55-61); and

circuitry for converting the substantially sinusoidal analog clock signal to the binary clock signal (Fig.2 element 70 and column 2 lines 41-51) such that the binary clock signal has a rate near an integer multiple of a rate of the analog clock signal (column 2 lines 52-67 and column 5 lines 1-10).

Note that the output of the look up table (Fig.2 element 40 output and Fig.4 element 85) represents discrete amplitude levels of the desired sine wave. The discrete nature of the time intervals, when discrete sine wave changes amplitude value, is the dominant limiting factor in the quality of the final square wave output signal. If this signal is directly converted to a square wave significant impairments will be present. These impairments will be evident as jitter in the time domain or phase noise in the frequency domain. Filter 60 removes the discrete time and amplitude properties to reduce the jitter by smoothing the signal (column 4 line 55 – column 5 lines 21).

- With regard to claim 3, Landry further discloses said filter comprises a low pass filter (Fig.4 element 60 and column 5 lines 22-23).
- With regard to claim 6, Landry further discloses wherein said circuitry for converting comprises a comparator (column 5 lines 46-47).
- With regard claim 16, which is a system claim related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 17, which is a system claim related to claim 3, all limitation is contained in claim 3. The explanation of all the limitation is already addressed in the above paragraph.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 4, 5, 8, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Landry (US 5,931,891) in view of Corry et al. (US 5,563,535).

- With regard claim 2, Landry discloses all of the subject matter as described in the above paragraph except for specifically teaching wherein said filter comprises a bandpass filter.

However, Corry et al. teaches wherein said filter comprises a bandpass filter (Fig.2 element 217 and column 5 lines 35-38).

It is desirable to include a variable bandpass filter at DSS output that performs an anti-alias function as well as reduces the excess noise outside a band of interest so that the DSS output clock signal quality is improved (column 5 lines 35-38). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the variable bandpass filter at DSS output as taught by Corry et al. to replace the band pass filter with a low pass filter into Landry's digital frequency synthesizer to sufficiently eliminate spurious signals from the output signal so that the DSS output clock signal quality is improved.

- With claim 4, Landry discloses all of the subject matter as described in the above paragraph except for specifically teaching wherein said memory stores digital data representing real and imaginary parts of a complex waveform.

However, Corry et al. teaches wherein said memory stores digital data representing real and imaginary parts of a complex waveform (column 6 lines 53-60). The Corry's reference, column 6 lines 53-60, teaches that the output of the LUT 207 is supplied to one input of a digital complex multiplier/accumulator (CMAC) 401. In a parallel data path, a complex digital baseband signal 403 is supplied to a second input of the CMAC 401. The output 409 of the CMAC 401, which is a stream of data representing the two quadrature phase components of the complex product (i.e., the modulated data stream), is then supplied to a

sideband select circuit 405 that generates the upper (or lower) sideband by combining the two quadrature components in-phase (anti-phase). It is inherent that the LUT output signal is a complex waveform or the stored digital data in LUT (memory) representing real and imaginary part of the complex waveform.

It is desirable that the memory stores digital data representing real and imaginary parts of a complex waveform in order to generate an extremely high frequency resolution clock so that the a DSS output clock signal quality is improved. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include a memory storing digital data representing real and imaginary parts of a complex waveform as taught by Corry et al. into Landry's ROM to improve the DSS output clock signal quality.

- With claim 5, all limitation is contained in claims 4 and 2. The explanation of all the limitation is already addressed in the above paragraph.
- With claim 8, Landry further discloses a phase-frequency detector comparing the input signal with a reference (Fig.2 and 4 elements 10, 20, and 30, column 1 lines 45-59, and column 4 lines 38-44).

Landry teaches a phase detector in Fig.1 for a PLL circuit and teaches a phase accumulator 20, phase accumulator register 30 for NCO circuit. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use phase accumulator and phase accumulator register as equivalence of a phase-frequency detector for their use in the communication art

and the selection of any of these known equivalents to calculate the phase error would be within the level of ordinary skill in the art.

Landry discloses all of the subject matter as described in the above paragraph except for specifically teaching a delta - sigma noise shaper for filtering at least a selected number of data bits output from said phase-frequency detector to generate selected bits of said memory address.

However, Corry et al. further discloses that the input circuitry comprises a delta - sigma noise shaper for filtering at least a selected number of data bits output (Fig.2 element 203 and column 5, lines 10-37) from said phase-frequency detector to generate selected bits of said memory address (column 1, line 28 – column 2, line 46 and column 5, lines 10-38).

It is desirable to include a delta - sigma noise shaper for filtering at least a selected number of data bits output from said phase-frequency detector to generate selected bits of said memory address. The reason for this is that normally, a DAC running at Nyquist sampling rates has a noise floor (power density) that is set by the size of the DAC (i.e., the number of bits that constitute the quantized waveform samples). However in the present invention, the sampling rate is increased without changing the data bandwidth (i.e., oversampling is performed), so that the noise density is decreased by the oversampling ratio, and excess noise can be filtered out by an anti-alias filter. In accordance with Corrys' reference, the oversampling is further utilized to simplify the filtering requirement by applying sigma-delta techniques to band-shape the

noise (attributable to the phase truncation error) away from a narrow band of interest so that the direct digital synthesizer (DDS) performance is improved (column 4 lines 48-62). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the phase accumulator circuit with delta-sigma shaper circuit as taught by Corry et al to replace that of phase accumulator as taught by Landry in order to improve DDS performance.

- With regard claim 18, which is a system claim related to claim 4, all limitation is contained in claim 4. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 19, which is a system claim related to claim 2, all limitation is contained in claim 2. The explanation of all the limitation is already addressed in the above paragraph.

6. Claims 7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Landry (US 5,931,891) in view of Dairi (US 6,515,526).

- With claim 7, Landry discloses all of the subject matter as described in the above paragraph except for specifically teaching wherein said circuitry for converting comprises a phase-locked loop.

However, Dairi teaches wherein said circuitry for converting comprises a phase-locked loop (Fig.1 elements 2-6 and column 4 lines 11-38). The Dairi's reference, column 4 lines 11-38, teaches a modulated signal generation section 6 with output connected to a PLL (Fig.1 elements 2-4), where the modulated

signal generation section 6 comprises a DSS and A/D as shown in Fig.3. The sine wave to digital wave conversion comprises A/D 64 and PLL 2-5. The detailed explanation is in column 4 line 48 – column 7 line 26.

It is desirable that t circuitry for converting comprises a phase-locked loop in order to reduce the phase fluctuation so that the quality of the generated system clock is improved. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to replace the comparator as taught in Landry's reference with a circuitry for converting comprising a phase-locked loop as taught by Daira in order to reduce the phase fluctuation so that the quality of the generated system clock is improved.

- With regard claim 20, which is a system claim related to claim 7, all limitation is contained in claim 7. The explanation of all the limitation is already addressed in the above paragraph.

7. Claims 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Landry (US 5,931,891) and Corry et al. (US 5,563,535) as applied to claims 2 and 4 above, and further in view of Dairi (US 6,515,526).

- With claim 9, Landry and Corry et al. disclose all of the subject matter as described in the above paragraph except for specifically teaching wherein said circuitry for converting comprises a phase-locked loop.

However, Dairi teaches wherein said circuitry for converting comprises a phase-locked loop (Fig.1 elements 2-6 and column 4 lines 11-38). The Dairi's reference, column 4 lines 11-38, teaches a modulated signal generation section

6 with output connected to a PLL (Fig.1 elements 2-4), where the modulated signal generation section 6 comprises a DSS and A/D as shown in Fig.3. The sine wave to digital wave conversion comprises A/D 64 and PLL 2-5. The detailed explanation is in column 4 line 48 – column 7 line 26.

It is desirable that the circuitry for converting comprises a phase-locked loop in order to reduce the phase fluctuation so that the quality of the generated system clock is improved. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to replace the comparator as taught in Landry's reference with a circuitry for converting comprising a phase-locked loop as taught by Daira in order to reduce the phase fluctuation so that the quality of the generated system clock is improved.

- With claim 15, Landry and Corry et al. disclose all of the subject matter as described in the above paragraph except for specifically teaching a circuitry for generating a memory index comprises a noise shaper for shaping noise output from said phase detector to reduce a size of said memory.

However, Corry et al. further teaches a circuitry for generating a memory index comprises a noise shaper for shaping noise output (Fig.1b element 115, Fig.2 element 203 and column 5, lines 10-37, and column 6 lines 30-44) from said phase detector to reduce a size of said memory (Fig.1b element 115, and column 2 lines 7-46). Refer to Fig.1b, the noise shaper receive m bits input from the accumulator and output p bits to the LUT (memory), where $p < m$. It is

inherent that the size of the LUT is reduced since it requires only p address bits instead of m address bits.

It is desirable that the circuitry for generating a memory index comprises a noise shaper for shaping noise output from said phase detector to reduce a size of said memory so that the quality of the generated system clock is improved. The noise shaping technique operates to increase noise suppression around the carrier frequency without significantly increasing the bandwidth of noise suppression. It would be desirable to increase the noise suppression bandwidth in order to allow more information to be conveyed for a given signal-to-noise ratio (S/N), and also to facilitate anti-alias filtering (column 2 lines 38-46). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to insert the noise shaping technique as taught by Corry et al. after the phase accumulator as taught by in Landry's reference with a circuitry for converting comprising a phase-locked loop as taught by Landry and Corry et al. in order to improve the noise suppression so that the quality of the generated system clock is improved.

8. Claims 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Landry (US 5,931,891) and Corry et al. (US 5,563,535) and Dairi (US 6,515,526) as applied to claim 9 above, and further in view of Raghavan et al. (US 5,859,605).

- With regard claim 14, Landry and Corry et al. and Dairi disclose all of the subject matter as described in the above paragraph except for specifically teaching wherein said digital to analog converter comprises a delta sigma converter.

However, Raghavan et al. teaches wherein said digital to analog converter comprises a delta sigma converter (Fig.1 element 16 and column 2 lines 13-53).

It is desirable that digital to analog converter comprises a delta sigma converter in order to improve the SNR in the signal spectrum (column lines 28-30) so that the quality of the generated system clock is improved. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to replace the DAC as taught in Landry's reference with a sigma-delta type DAC as taught by Raghavan et al. in order to improve the SNR in the signal spectrum (column lines 28-30) so that the quality of the generated system clock is improved.

Allowable Subject Matter

9. Claims 10-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2634

Ted M. Wang

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